Exhibit K

MacInnis 7,512,752 Applied to Representative Renesas Components and Infotainment Systems and Automobiles Incorporating Those Components

This claim chart compares independent claim 1 of U.S. Patent No. 7,512,752 ("the MacInnis '752 patent") to Renesas's R-Car H3 system on a chip ("SoC").

On information and belief, Renesas's R-Car H3 SoC is representative of other Renesas infotainment and high-end car information system SoCs having similar functionality ("Accused Renesas Infotainment SoCs"), including, and without limitation, the Renesas R-Car H2 and the Renesas R-Mobile A1. *See* Declaration of Dr. Joseph Havlicek ("Ex. 67, Havlicek Decl."), ¶¶ 16.

The R-Car H2 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser No. 112905, that form Accused Toyota Navigation units, including Camry Navigation System with WiFi Hotspot (86840-06011).

The R-Mobile A1 SoC is incorporated in downstream products, including without limitation, at least Denso Ten, formerly Fujitsu Ten, head units, such as Ser. Nos. MMA00002, MM910406, and MM100046, which are incorporated in Accused Toyota Navigation units, including Camry Receiver (86804-06180), Corolla Nav System Kit (86804-02070), and Camry Navigation System Receiver (86804-06100).

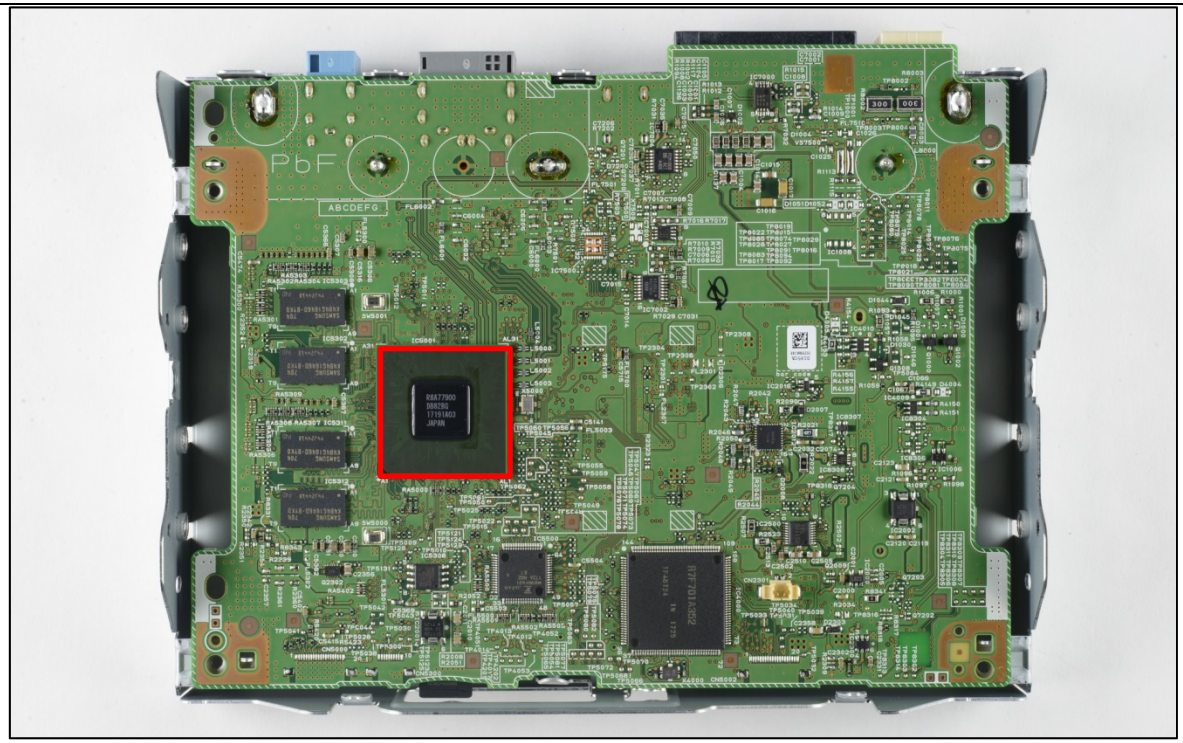
On information and belief, the Accused Renesas Infotainment SoCs, and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs, infringe directly, indirectly, and/or under the doctrine of equivalents at least claim 1 of the MacInnis '752 patent.

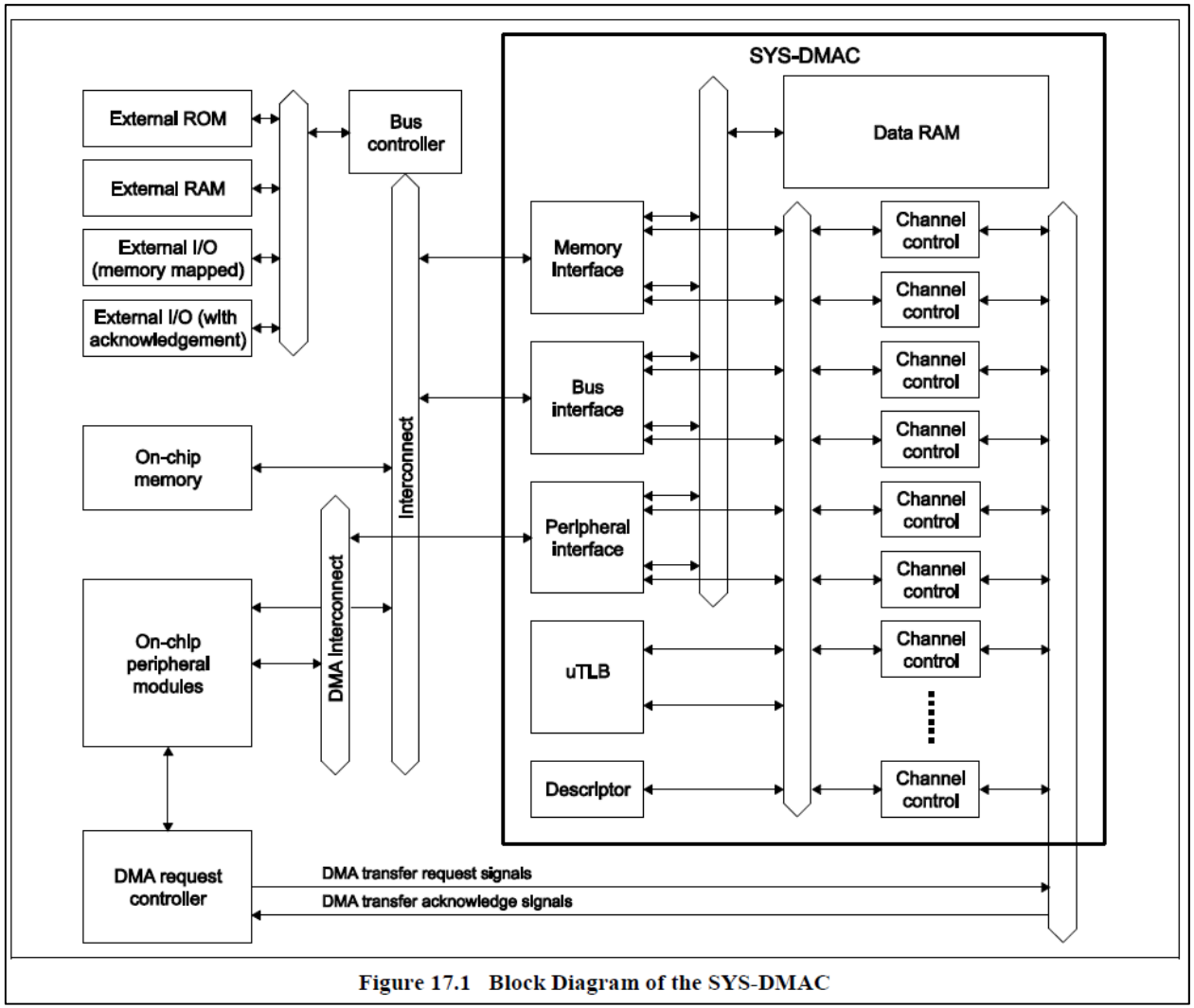
Claim - U.S. Patent No. 7,512,752 (MacInnis)	**Application of Claim Language to Accused Products**
Claim 1	
A memory access unit for accessing data for a module, said memory access unit comprising:	To the extent that the preamble is deemed limiting, the Accused Renesas SoCs and downstream products include a memory access unit for accessing data for a module. At least the Fujitsu Ten (MM910406) head unit, which is included in at least the Toyota Corolla Navigation System Kit (26187), includes a Renesas R-Mobile A1 SoC (highlighted in yellow).

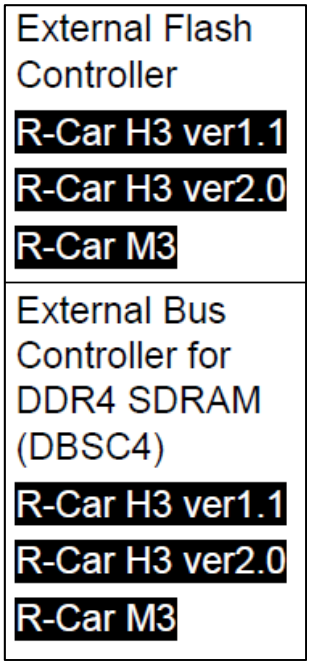
	 TOYOTA 86804-02070 FUJITSU TEN 139000-0690B101 ASSEMBLED IN MEXICO MM910406 MANUFACTURER: FUJITSU TEN LIMITED ADDRESS: 2-28, Gosho-dori 1-chome Hyogo-ku, Kobe 652-8510, JAPAN MANUFACTURED: September 2015 Complies with 21 CFR Chapter 1, Subchapter J. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. HD Radio Technology manufactured under license from iBiquity Digital Corporation. U.S. and Foreign Patents. HD Radio™ and the HD, HD Radio, and "Arc" logos are proprietary trademarks of iBiquity Digital Corp. AM 530 to 1710kHz FM 87.75 to 107.9MHz FCC ID: BABFT0044C IC: 2024B-FT0044C Model: FT0044C RCPFUFT12-1493 TYPE: FT0044D microSDHC Logo is a trademark of SD-3C, LLC. MM910406 86804-02070

At least the Panasonic (AT1604) head unit, which is included in at least the Toyota Camry Navigation System (301378), includes a Renesas R-Car H2 SoC (highlighted in red).

	 Model No 86840-06011 Ref. No CN-SS87N0*XA Set No AT1604 CE DC 12V Negative Ground Panasonic Automotive Systems de Mexico S.A. de C.V. Made in Mexico Serial No 112905 "This system contains software that is licensed to Panasonic Corporation by one or more third parties pursuant to license agreement(s). Any removal, reproduction, reverse engineering or other unauthorized use of the software from this system in violation of the license agreement(s) is strictly prohibited."

	 The Renesas R-Car H3 SoC includes a Direct Memory Access Controller for System (SYS-DMAC), which is a memory access unit for accessing data for a module. This LSI includes a direct memory access controller for system (SYS-DMAC). The SYS-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules. Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-1.
an output port for providing access requests for lists of addresses in a memory over a link to a	The Renesas R-Car H3's Direct Memory Access Controller for System (SYS-DMAC) includes an output port for providing access requests for lists of addresses in a memory over a link to a memory controller. The SYS-DMAC's memory interface includes output ports for providing access requests for lists of addresses in a memory over an interconnect.

memory controller; and	 **Figure 17.1 Block Diagram of the SYS-DMAC** Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-2. The SYS-DMAC provides access requests for lists of addresses to memory controllers such as the external flash memory controller and the DDR4 SDRAM memory controller.



Ex. 68 – Renesas R-Car H3/M3 Device Manual at 1-3.

The SYS-DMAC's output port provides for access requests for lists of addresses.

17.3.5 Transmission Flow

Set the transfer conditions as required in the following registers:

DMA source address register (DMASAR), DMA destination address register (DMADAR), DMA transfer count register (DMATCR), DMA Channel control register (DMACHCR), DMA operation register (DMAOR) and DMA extended resource selector (DMARS)

Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-90.

<table>
<tr>
<td></td>
<td>
17.2.17 DMA Destination Address Registers 0 to 47 (DMADAR_0 to DMADAR_47)
<table>
<tr><td>R-Car H3</td><td>R-Car M3</td></tr>
<tr><td>√</td><td>√</td></tr>
</table>
DMADAR is 32-bit readable/writable register that specify the destination address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next destination address.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-54.

17.2.20 DMA Transfer Size Registers 0 to 47 (DMATSR_0 to DMATSR_47)
<table>
<tr><td>R-Car H3</td><td>R-Car M3</td></tr>
<tr><td>√</td><td>√</td></tr>
</table>
DMATSR is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the read transfer size.
Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-56.
</td>
</tr>
<tr>
<td>a queue for queuing the access requests for the lists of addresses.</td>
<td>
The Renesas R-Car H3's Direct Memory Access Controller for System (SYS-DMAC) includes a queue for queuing the access requests for the lists of addresses.

For example, the SYS-DMAC includes 48 channels for DMA transfers and the 48 channels keep the destination address lists queued as the SYS-DMAC processes the requests individually.

17.2.17 DMA Destination Address Registers 0 to 47 (DMADAR_0 to DMADAR_47)
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	Ex. 68 – Renesas R-Car H3/M3 Device Manual at 17-54.